1.	Title of the course	Testing and Verification of VLSI Systems
2.	Course number	CS526L
3.	Structure of credits	3-0-0-3
4.	Offered to	PG
5.	New course/modification to	Modification To CS5227/14
6.	To be offered by	Department of Computer Science and Engineering
7.	To take effect from	July 2022
8.	Prerequisite	CoT
9.	**Course Objective(s):** To introduce the reliablity aspects of the VLSI design and develop algorithms for testing and verification of the large systems.	
10.	**Course Content:** Fundamentals of testing: VLSI design process, defect and fault model, fault simulation, test generation algorithm, test-ability measures, test economy, test equipment; Design for test-ability: scan designs, built-in-self-test (BIST), boundary-scan architecture, SoC test; Delay test: fault model, pattern generation, scan-based delay test, small delay defects; Memory test: functional fault model, memory test algorithm, memory BIST, diagnosis; Test optimization: test compression, power-aware test; Verification: dynamic verification, formal equivalence checking, binary decision diagram, finite automata, formal property checking, temporal logic, timing verification, hardware emulation.	
11.	**Textbook(s):** 1. Bushnell M L and Agrawal V D, *Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits*, 1st Edition, Springer (2002).	
12.	**Reference(s):** 1. Fujita M, Ghosh I and Prasad M, *Verification Techniques for System-Level Design*, 1st Edition, Morgan Kaufmann (2008). 2. Huth M and Ryan M, *Logic in Computer Science*, 2nd Edition, Cambridge University Press (2004). 3. Jha N and Gupta S, *Testing of Digital System*, 1st Edition, Cambridge University Press (2013). 4. Wang L T, Stroud C and Touba N, *System-on-Chip Test Architectures: Nanometer Design for Testability*, 1st Edition, Morgan Kaufmann (2007).	