1.	Title of the course	Digital Systems Laboratory
2.	Course number	EE206P
3.	Structure of credits	0-0-3-2
4.	Offered to	UG
5.	New course/modification to	Modification To CS/EE2191/8
6.	To be offered by	Dept. of Electrical Engineering/Dept. of Computer Science and Engineering
7.	To take effect from	July 2022
8.	Prerequisite	Nil
9.	**Course Objective(s):** To provide the methods and techniques for hands-on experience in designing digital logic circuits and systems.	
10.	**Course Content:** Design of logic gates using logic families: Diode Logic (DL), Resistor-Transistor Logic (RTL), Diode-Transistor Logic (DTL), TransistorTransistor Logic (TTL), Emitter Coupled Logic (ECL), Integrated Injection Logic (IIL) and CMOS logic; Arithmetic Logic Unit (ALU) Design: Multiplexers, Encoders, Decoders, Ripple Carry and Carry Look-ahead Adder, Subtractor, Multiplier and Divider; Sequential Logic Design: Latches, Flip-fops, Clocking and Timing Analysis; Registers and Counters: Shift Registers, Universal Shift Register, Synchronous and Asynchronous Counters, and Buffers/Queues State Machine and Controller Design: Finite State Machine and Transition Diagram, Moore's Machine and Mealy's Machine, State Machine as Controller and Algorithmic State Machine (ASM); Practical Application Design: Design and use of semiconductor IP blocks.	
11.	**Textbook(s):** 1. Mano M M and Ciletti M D, *Digital Design: with Introduction to the Verilog HDL, VHDL, and SystemVerilog*, Pearson (2008). 2. Ashenden P J , Digital Design (Verilog): An Embedded Systems Approach Using Verilog, Morgan Kaufmann (2007).	
12.	**Reference(s):** 1. Palnitkar Samir, *Verilog HDL: A Guide to Digital Design and Synthesis*, Pearson Publishing (2003).	