1.	Title of the course	FPGA Laboratory
2.	Course number	EE536P
3.	Structure of credits	0-0-3-2
4.	Offered to	PG
5.	New course/modification to	Modification To EE5296/16
6.	To be offered by	Department of Electrical Engineering
7.	To take effect from	July 2022
8.	Prerequisite	Nil
9.	**Course Objective(s):** To introduce the concepts related to the Hardware Description Language (HDL) and Field Programmable Gate Arrays (FPGA). To demonstrate the implementation of real time applications using HDL and FPGA.	
10.	**Course Content:** Introduction to Hardware Description Language (HDL); Design of floating point arithmetic unit for addition, multiplication and division; Fast multiplication; Fast division; CORDIC, Fast Fourier Transform (FFT); FIR filter design and error correcting codes; Authenticated encryption using AES and SHA-256; RS232 serial port communication between PC and FPGA; Simple processor design.	
11.	**Textbook(s):** 1. Koren I, *Computer Arithmetic Algorithms*, 2nd Edition, Universities Press (2005). 2. Peter J A, *Digital Design (Verilog): An Embedded Systems Approach Using Verilog*, 1st Edition, Morgan Kaufmann (2007).	
12.	**Reference(s):** 1. Morris M M and Michael D C, *Digital Design With an Introduction to the Verilog HDL, VHDL, and SystemVerilog*, 6th Edition, Pearson Education (2018). 2. Yamin L, *Computer Principles and Design in Verilog HDL*, 1st Edition, Wiley (2015).	